CLAIMS

We claim:

1. A method of operating a programmable logic device comprising:

enabling resources of the programmable logic device being used in a circuit design implemented by the programmable logic device; and

de-coupling one or more unused or inactive resources of the programmable logic device which are not being used in the circuit design from one or more power supply terminals.

2. The method of Claim 1, wherein the one or more power supply terminals comprise a positive voltage supply terminal.

3. The method of Claim 1, wherein the one or more power supply terminals comprise a ground voltage supply terminal.

4. The method of Claim 1, wherein the step of de-coupling is performed in response to configuration data bits stored by the programmable logic device.

5. The method of Claim 4, further comprising defining the configuration data bits during design time of the programmable logic device.

6. The method of Claim 4, wherein the step of de-coupling is also performed in response to user controlled signals.

7. The method of Claim 6, further comprising defining the user controlled signals during run time of the programmable logic device.

8. The method of Claim 7, further comprising generating the user controlled signals in response to operating conditions of the programmable logic device during run time.

9. The method of Claim 1, wherein the step of de-coupling is performed in response to user controlled signals.

10. The method of Claim 9, further comprising defining the user controlled signals during run time of the programmable logic device.

11. The method of Claim 10, further comprising generating the user controlled signals in response to operating conditions of the programmable logic device during run time.

12. The method of Claim 11, wherein the step of generating comprises generating the user controlled signals with resources of the programmable logic device.

13. The method of Claim 1, wherein the step of decoupling comprises turning off at least one transistor coupled between the one or more unused or inactive resources and the one or more power supply terminals.

14. The method of Claim 1 further comprising dividing the programmable logic device into a plurality of programmable logic blocks, wherein at least one of the programmable logic blocks includes at least a portion of the one or more unused or inactive resources.

15. A method of operating a programmable logic device comprising:

enabling resources of the programmable logic device being used in a circuit design implemented by the programmable logic device; and

regulating a supply voltage applied to unused or inactive resources of the programmable logic device which are not being used in the circuit design.

16. The method of Claim 15, wherein the step of regulating the supply voltage comprises lowering the supply voltage to a predetermined level.

17. The method of Claim 15, wherein the step of regulating is performed in response to configuration data bits stored by the programmable logic device.

18. The method of Claim 17, further comprising defining the configuration data bits during design time of the programmable logic device.

19. The method of Claim 17, wherein the step of regulating is also performed in response to user controlled signals.

20. The method of Claim 19, further comprising defining the user controlled signals during run time of the programmable logic device.

21. The method of Claim 20, further comprising generating the user controlled signals in response to operating conditions of the programmable logic device during run time.

22. The method of Claim 15, wherein the step of regulating is performed in response to user controlled signals.

23. The method of Claim 22, further comprising defining the user controlled signals during run time of the programmable logic device.

24. The method of Claim 23, further comprising generating the user controlled signals in response to operating conditions of the programmable logic device during run time.

25. The method of Claim 24, wherein the step of generating comprises generating the user controlled signals with resources of the programmable logic device.

26. A programmable logic device comprising:

a first voltage supply terminal configured to receive a first supply voltage;

a plurality of programmable logic blocks, each programmable logic block comprising one or more resources of the programmable logic device; and

a plurality of first switch elements, wherein each first switch element is coupled between one of the programmable logic blocks and the first voltage supply terminal.

27. The programmable logic device of Claim 26, further comprising:

a second voltage supply terminal configured to receive a second supply voltage; and

a plurality of second switch elements, wherein each second switch element is coupled between one of the programmable logic blocks and the second voltage supply terminal.

28. The programmable logic device of Claim 26, further comprising a control circuit coupled to the plurality of first switch elements, wherein the control circuit is configured to provide a plurality of control signals for controlling the plurality of first switch elements.

29. The programmable logic device of Claim 28, wherein the control circuit comprises a plurality of configuration memory cells configured to store a corresponding plurality of

configuration data values, wherein the control circuit provides the plurality of control signals in response to the plurality of configuration data values.

30. The programmable logic device of Claim 29, wherein the control circuit further comprises a plurality of user control terminals configured to receive a corresponding plurality of user control signals, wherein the control circuit further provides the plurality of control signals in response to the plurality of user control signals.

31. The programmable logic device of Claim 28, wherein the control circuit comprises a plurality of user control terminals configured to receive a corresponding plurality of user control signals, wherein the control circuit provides the plurality of control signals in response to the plurality of user control signals.

32. The programmable logic device of Claim 26, wherein each first switch element comprises a transistor.

33. A programmable logic device comprising:

a first voltage supply terminal configured to receive a first supply voltage;

a plurality of programmable logic blocks, each programmable logic block comprising one or more resources of the programmable logic device; and

a plurality of voltage regulators, wherein each voltage regulator is coupled between one of the programmable logic blocks and the first voltage supply terminal.

34. The programmable logic device of Claim 33, further comprising a control circuit coupled to each of the voltage regulators, wherein the control circuit is configured to provide a plurality of control signals for controlling the plurality of voltage regulators.

35. The programmable logic device of Claim 34, wherein the control circuit comprises a plurality of configuration memory cells configured to store a corresponding plurality of configuration data values, wherein the control circuit provides the plurality of control signals in response to the plurality of configuration data values.

36. The programmable logic device of Claim 35, wherein the control circuit further comprises a plurality of user control terminals configured to receive a corresponding plurality of user control signals, wherein the control circuit further provides the plurality of control signals in response to the plurality of user control signals.

37. The programmable logic device of Claim 34, wherein the control circuit comprises a plurality of user control terminals configured to receive a corresponding plurality of user control signals, wherein the control circuit provides the plurality of control signals in response to the plurality of user control signals.